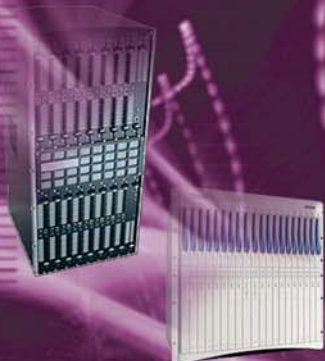


TeraSync

The complete NE (Network Element) BITS/SSU (Building Integrated Timing Supply/Synchronization Supply Unit) interface solution, providing the host with a unique tool that fulfills all of the user's timing distribution & message handling requirements.

BITSync is also a tool for a non-external timed NE, where no BITS/SSU is available, enabling automatic SSM (Synchronization Status Message) based timing reference switching.

**Environmental Friendly
- RoHS Compliance**



 **TeraSync**



BITSync™-TS-810A

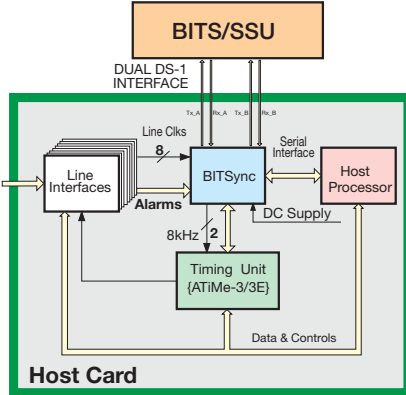
Embedded OEM BITS/SSU Interface Module for Network Synchronization and Timing Source Management.

Features

- Telcordia: GR-1244-CORE, GR-253-CORE and GR-378-CORE
ANSI: T1.101 and T1.403
ITU-T: G.810/G.811/G.812/G.814 and G.703/G.704/G.781
- External Timing, Line Timing, Through Timing, Loop Timing and Hold Over timing modes support
- Message Pass Through and Threshold AIS Generation mode support
- 3.3 V power supply
- Automatic timing reference switching based on LOS frequency offset and SSM messages (first and second generation) processing
- Up to eight timing references in the line/ through timing mode
- Two DS1 interfaces in the external timing mode
- T1/E1 selectable
- Manual timing reference switching command:
 - Manual, Forced Switch, Clear Forced, Lock Out and Clear Lock Out commands support
- Automatic or manual timing mode switching
- Automatic or manual switching of the derived DS1 reference based on:
 - SSM automatic switching
 - Continuous reference monitoring: frequency offset and LOS
 - Manual, Forced Switch, Clear Forced, Lock Out, and Clear Lock Out commands support
- Automatic alarm processing
- I²C, UART serial host processor interface
- Complete interface to Terasync's ATiMe Stratum 2,3 and 3E models

Description

BITSync is an embedded OEM interface module handling SSMS (Synchronization Status Messages) and Interface functions to BITS/SSU (Building Integrated Timing Supply/Synchronization Supply Unit). The BITSync is designed to fulfill all of the required interfacing between the NE (Network Element) and the on-site BITS/SSU and is an essential component of the managed timing distribution telecom network.



Line Interface
OC-N
T1/T3
E1/E3

Within the NE, the BITSync module provides all of the required hardware and software functions compliant to the following international standards:

- Telcordia GR-1244-CORE, GR-253-CORE, GR-378-CORE and GR-436-CORE
- ANSI T1.101 and T1.403
- ITU-T G.810/G.811/G.812 and ITU-T G.703/G.704/G.781

The BITSync module supports all possible timing modes: external, line, through and loop timing modes. It also provides the network manager with a very flexible, yet powerful tool for automatic or manual reference selection and switching. The BITSync can perform automatic reference switching based on the incoming line's SSMS (Synchronization Status Messages) and/or the real time switching criteria supplied by the user.

The BITSync also provides an SSM - BITS/SSU interface for handling both, BITS/SSU with SSM support capabilities and BITS/SSU without SSM support capabilities

In the cases in which the BITS/SSU supports the SSM mechanism, the BITSync shall provide a transparent transfer to the incoming messages from the line interface to the BITS/SSU (this mode of message transferring is called "message pass through" mode). In the case in which the BITS/SSU does not support the SSM mechanism, the BITSync is capable of alerting the BITS/SSU by generating an AIS alarm to the BITS/SSU (this message transferring system is called "Threshold AIS generation mode").

BITSync-clock unit: The BITSync supplies the highest quality references available (two 8 KHz frequencies) to the on-site clock unit, provided either from the BITS (when working in an external timed NE) or from the line interface (when working in a line-timed NE). A serial interface (UART or I²C) provides the user with an effective and user-friendly real-time control over the BITSync's reference selection and timing distribution criteria.

Specifications

BITSync-BITS:

Two DS-1/E1 channels (8 lines)_-Channel A/B:
Inputs-RRING_A / B ,RTIP_A / B.....DS1 SIGNALS
Outputs-TRING_A / B ,TTIP_A / B...DS1 SIGNALS

BITSync-Line:

Inputs:
8 line clocks L_Clk_1-8.....8khz or 1.544/2.048 MHz
8 line clocks alarms L_Alrm_1-8.....High/Low Indication.

BITSync-Host:

A serial communication interface ...UART / I²C
Bi-directional alarm, status and control indications

BITSync-Unit Clock:

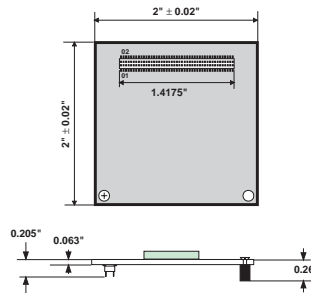
Inputs:
Std_clkfree-running clock

Outputs:

Ref_clk, Alt_ref_clk, primary
and alternate reference clock.....8KHz
Sync_out.....1.544 / 2.048 MHz
Signal levelLVTTTL (TTL tolerable)
Power supply.....3.3 VDC

Input and Output Reference Signal Characteristics:

Jitter Generation	Telcordia:GR-1244-CORE, GR-253-CORE, ANSI T1. 101
Wander Generation and Tolerance.....	Telcordia: GR-1244-CORE, GR-253-CORE,ANSI T1. 101
MTIE	Telcordia: GR-1244-CORE, GR-253-CORE,ANSI T1. 101
TDEV.....	Telcordia: GR-1244-CORE, GR-253-CORE,ANSI T1. 101



TeraSync Inc.
149 Mill Street
Burlington, MA 01803
USA
Tel: (781) 273-2551
Fax: (781) 273-0521

TeraSync Ltd.
14 Shabazi Street
P. O. Box 160
Yehud 56000, Israel
Tel: +972 3 536-0202
Fax: +972 3 536-0020

<http://www.terasync.net> e-mail: info@terasync.net