

TeraSync



Ultra Small:  
1.2"x1.2"



- *<1pSec jitter RMS*
- *Ultra small: 1.2"x1.2"*
- *Fully compliant with the international standards of Telcordia GR-253-CORE and ITU-T G.709*

Environmental Friendly  
- RoHS Compliance

## SLC™-Small Line Card

Small, High Speed, Hitless and Ultra Low Jitter OEM Timing Module for OC-3 through OC-192 Line Interface Cards

### Applications

Advanced timing and synchronization solution for:

- Core and access IP switches
- DWDM, SONET and SDH, cross-connect, ADM and transmission products
- Broadband, multi-service access products

- Reference and 8Khz composite clock inputs available
- Revertive and non-revertive function, user selectable
- JTAG boundary support
- Telcordia: GR-253-CORE and ITU-TG.709 compliant

### Key Features

- Single high frequency VCXO
- Small size: 1.2"x1.2"
- 3.3 V technology
- Three reference inputs in LVPECL or TTL levels (2+1 loop-back)
- Two high frequency outputs in LVPECL levels
- One 8 KHz output in TTL level
- Control and status lines
- Hitless switching between reference inputs
- Simple board-to-board connector for easy mounting
- 400 pSec phase-shift adjustment function

- A very high frequency output clock for OC-N framers and phys
- Ultra low phase jitter reference clock, below 1 picosecond RMS
- Reference redundant operation: Hitless switch-over between two external input reference signals - automatic or manual
- Continuous input reference monitoring of the two external references
- FEC frequencies support
- 8 KHz output signal synchronized with the main output reference signal
- Compatible with all common OC-N and STM-N framers and PHYs on the market.
- Flexible architecture adaptable to user's applications
- Seamless integration with TeraSync's ATiMe Stratum 2, 3 and 3E modules

SDH

SONET

DWDM

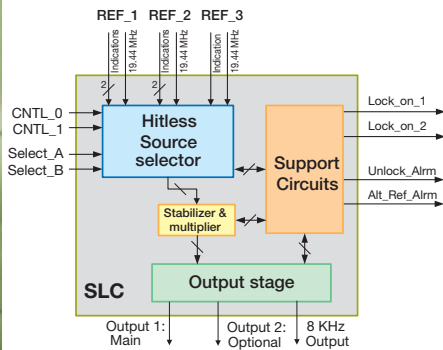


## Description

The SLC (Small Line Card) is a 1.2"x1.2", ultra-small OEM timing module integrated into line interface cards of telecom network equipment such as long haul, core and access switches, cross connects, transport equipment, SONET/LAN convergence and so forth. The SLC provides all of the timing functions wherever OC-N interfaces are used and installed in conjunction with other Stratum clocks such as TeraSync's Stratum 2, 3, and 3E product lines. The SLC provides a full timing solution for equipment incorporating an OC-N interface, complying with Telcordia GR-253-CORE and ITU-T Rec. G709.

The SLC meets the relevant performance and functional requirements necessary for timing modules installed in line interface cards.

The SLC Block Diagram:



### Main Functions:

**Timing:** The SLC generates high frequency timing signals needed to drive the high-speed OC-N framers and PHYs. The output-timing signal is enslaved to the active input reference clock traceable to the TU (Timing Unit) output (derived from the central timing card/s).

**Phase noise and jitter reduction:** The SLC generates a timing signal with very low phase noise and jitter to drive the OC-N chipsets. It reduces the jitter and noise originating from:

- A reference that complies with the Stratum 3 & 3E standards.
- Accumulated noise in the backplane.

**Hitless switch-over between references:** The SLC monitors the two main input references. When it detects a malfunctioning reference, it activates, either manually or automatically, the process of hitless switch-over to an alternative reference, according to the switching criteria defined by the internal state machine.

**400pSec phase shift adjustment:** This feature prevents time error accumulation resulting from input switch-over.

### Management functions:

The SLC's internal logic supports several management functions. These functions provide both, the information and the means to manage the SLC through the host. The module's status indicators monitor each input timing reference signal. Based on this information, the switchover between references is determined. Manual and auto setting is user selectable and enables the application of the module's revertive/non-revertive function.

### Modes of operation:

- Enslaved to external reference 1
- Enslaved to external reference 2

### The secondary output provides:

- A binary division of the main output down to 19.44 MHz.
- An identical reference to the main output

## Specifications

### Input Signal

REF_1, REF_2 .....	19.44 MHz (or 19MHz/8KHz CC)
Signal level .....	TTL or LVPECL
REF_3 .....	19.44 MHz
Signal level .....	TTL
Time reference characteristics .....	Stratum 2, 3 or 3E, SMC or SEC
Status signals .....	Two per each REF input
Jitter tolerance .....	Telcordia: GR-253-CORE, ITU-T: G.813

### Output Signal

Output 1(Main) .....	77.76, 155.52, 622.08, 669.932 MHz or others
Output 2 (Secondary) .....	Main output divided by 1, 2, 4 or 8
Signal level .....	LVPECL
8KHz Output .....	Phase aligned with Main Output

### Output Reference Signal Characteristics

#### Jitter generation:

622/666 MHz modules .....	Less than 1 picoSec RMS at 50 KHz through 80 MHz
77/155 MHz modules .....	Less than 1 picoSec RMS at 12 KHz through 20 MHz

Wander generation .....

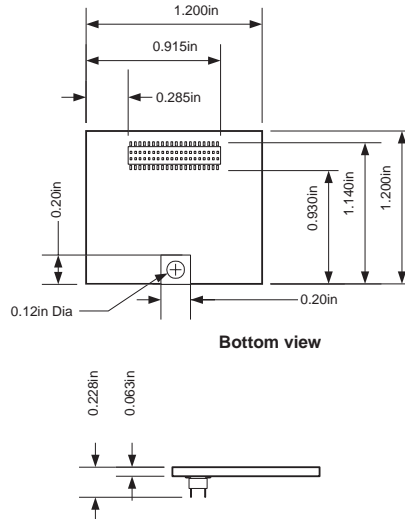
TDEV and MTIE .....

### PLL characteristic

Pull in range .....

### Power supply

Input voltage .....



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